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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/079,775	02/19/2002	Marina V. Plat	D900D/1368D	9123

7590 08/05/2003

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EXAMINER
LEE, HSIEN MING

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 08/05/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/079,775	PLAT ET AL.	
	Examin r	Art Unit	
	Hsien-Ming Lee	2823	

-- The MAILING DATE of this communication appears on the cov r sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 May 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 13-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 13-17* is/are rejected.

7)☒ Claim(s) *1 and 13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Remarks

1. The objection to the title is still sustained because the objection has not been properly responded. The new title " Method of Making a Semiconductor Device" is too broad to reflect the instant invention. Changing into " A Method for Reducing ARC layer Removal During Removal of Photoresist" is suggested, i.e. deleting " and System" as in originally filed title.

2. Claims 1-6 and 13-17 are pending in the application.

Claim Objections

3. Claim 1 is objected to because of the following informalities: in-consistent term, i.e. in step (e) "patterning a second resist layer, the resist layer...." should be – patterning a second resist layer, the **second** resist layer --. Claim 13 (line 5)," an layer of SiON" should be – **a** layer of SiON." Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-6 and 13-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Plat et al. (US 6,265,751) in view of Chung et al. (US 6,184,142) and applicants' admitted prior art (hereinafter referred as "AAPA").

In re claim 1-3 and 6, Plat et al., in Figs. 4A-4B, 5, 6A-6D and related text, teach the claimed method providing a semiconductor device, the semiconductor including a first layer 212 desired to be etched, the method comprising the steps of:

(a) providing, by depositing, an antireflective coating (ARC) layer 214, wherein the ARC layer 214 comprises a layer of SiON having a thickness of less than about 500 Angstroms, or three hundred Angstroms plus or minus no more than approximately ten percent, deposited on the first layer 212 (Fig.6A and col. 5, lines 55-57; col. 6, lines 51-56);

(b) patterning a resist layer (not shown, col. 6, lines 20-22), the resist layer including a pattern having a plurality of apertures therein for etching a first portion (i.e. the portion located at 202) of the first layer 212 (Fig.6C);

(c) etching the first portion of the first layer 212 (Figs. 6B-6C);

(d) removing the first resist layer, the ARC layer 214 being resistant to an etchant (col. 6, lines 29-30);

(e) patterning a second resist layer (not shown, col. 6, lines 33-34), the resist layer including a pattern having a plurality of apertures therein for etching a second portion (i.e. the portion located at 204) of the first layer 212; and

(f) etching the second portion of the first layer 212 (Figs.6C-6D).

In re claims 13-17, Plat et al. teach the claimed method of providing a semiconductor device including first 202 and second 204 regions, having , respectively, first (i.e. memory cells) and second (i.e. logic circuits) types of circuit structures, the method comprising :

- depositing a first layer 212 on a substrate 210 (Fig.6A);

- depositing a layer of SiON 214 (i.e. ARC) on the first layer 212 (Fig.6A), wherein the SiON layer 214 has a thickness of less than about 500 Angstroms or about 300 Angstroms or between about 270 and about 300 Angstroms (col. 5, lines 55- 60);
- depositing a first resist layer (not shown) on the SiON layer 214;
- patterning the first resist layer for etching the first layer 212 in a first region 202 of the semiconductor device;
- etching the first layer 212 in the first region 202 of the semiconductor device (Fig. 6C);
- removing the first resist layer;
- depositing a second resist layer (not shown) on the SiON layer 214;
- patterning the second resist layer for etching the first layer 212 in the second region 204 of the semiconductor device;
- etching the first layer 212 in the second region 204 of the semiconductor device (Fig. 6D);
- removing the second resist layer; and
- removing the SiON layer 214.

In contrast, Plat et al. do not teach utilizing plasma etch for removing the resist layer.

However, plasma etch has been widely used for the removing purpose, as evidenced by Chung et al. (col. 4, lines 44-48), wherein a forming gas (O2) is used and the ARC is resistant to the O2 plasma etch.

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time the invention was made, to utilize the plasma etch as taught by Chung et al. in the method of Plat, since by doing so it would satisfactory remove the resist layer.

In re claim 4, Plat et al. in view of Chung et al. teach removing the resist layer utilizing a plasma etch with a plasma including a forming gas, as stated above, but do not expressly teach that the plasma includes four percent of the forming gas.

However, the selection of the percentage of the forming gas is obvious because it is a matter of determining optimum process condition by routine experimentation with a limited number of species. In re Jones, 162 USPQ 224 (CCPA 1955)(the selection of optimum ranges within prior art general conditions is obvious) and In re Boesch, 205 USPQ 215 (CCPA 1980)(discovery of optimum value of result effective variable in a known process is obvious). In such a situation, applicants must show that the particular range is critical, generally by showing that that claimed range achieves unexpected results. See M.P.E.P. 2144.05 III. In fact, the originally filed specification does not demonstrate any criticality and/or novelty as to why the forming gas has to be four percent.

In re claim 5, Plat et al. in view of Chung et al. substantially teach the claimed method, including removing the resist layer utilizing a plasma etch, but do not expressly teach providing a wet preclean after the plasma etching step (d).

However, AAPA teaches providing the ARC layer 52; patterning a resist layer 53; etching a first layer 51 and the ARC layer 53; and removing the resist layer 53 followed by a wet etch (page 2, lines 9-11).

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time the invention was made, to perform the wet preclean (i.e. wet etch) as taught by AAPA after removing the resist layer in the method of Plat in view of Chung, since by doing so it would clean the residues from the plasma etching (page 2, lines 10-11, AAPA), which, in turn, would benefit the critical dimension of the device.

6. Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chung et al. (US 6,184,142) in view of AAPA and Li et al. (US 6,423,628).

In re claims 1-3 and 6, Chung et al., in Figs. 6A-6F and related text, teach the claimed method providing a semiconductor device, the semiconductor including a first layer 113/116/112 desired to be etched, the method comprising the steps of:

(a) providing, by depositing, an antireflective coating (ARC) layer 114 (Fig. 3C), which is a SiON having antireflective properties (col. 4, lines 30-32);

(b) patterning a resist layer 130, the resist layer 130 including a pattern having a plurality of apertures therein for etching a first portion (i.e. the portion where a dual damascene opening to be formed) of the first layer 113/116/112 (Fig. 6A);

(c) etching the first portion of the first layer 113/116/112 (Figs. 6C);

(d) removing the resist layer 130 utilizing a plasma etch with O_2 plasma, the ARC layer 14 being resistant to the plasma etch (O_2 plasma) (Figs. 6A-6B);

(e) patterning a second resist layer 131, the resist layer 131 including a pattern having a plurality of apertures therein for etching a second portion of the first layer 113/116/112 (Fig.6D); and

(f) etching the second portion of the first layer 113/116/112, i.e. forming the opening on the right as shown in Fig. 6F (Figs. 6E-6F).

In contrast, Chung et al. do not teach that the ARC layer has a thickness of less than about 500 Angstroms (claim 1) or 300 Angstroms plus or minus thirty Angstroms (claim 6).

However, the selection of the ARC layer thickness is obvious because it is a matter of determining optimum process condition by routine experimentation with a limited number of species. In re Jones, 162 USPQ 224 (CCPA 1955)(the selection of optimum ranges within prior art general conditions is obvious) and In re Boesch, 205 USPQ 215 (CCPA 1980)(discovery of optimum value of result effective variable in a known process is obvious). For example, the thickness is a consideration of optimizing an antireflective properties for etching purpose, as evidenced by AAPA, wherein the ARC layer is typically 300 Angstroms plus or minus thirty Angstroms (pages 1-2).

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time the invention was made, to select a desired ARC thickness as taught by AAPA in the method of Chung et al., since by this manner it would provide a suitable antireflective property for etching purpose.

In re claim 4, Chung et al. in view of AAPA teach removing the resist layer utilizing a plasma etch with a plasma including a forming gas (i.e. O_2) but do not expressly teach that the plasma includes four percent of the forming gas.

However, the selection of the percentage of the forming gas is obvious because it is a matter of determining optimum process condition by routine experimentation with a limited number of species. In re Jones, 162 USPQ 224 (CCPA 1955)(the selection of optimum ranges

within prior art general conditions is obvious) and In re Boesch, 205 USPQ 215 (CCPA 1980)(discovery of optimum value of result effective variable in a known process is obvious). In such a situation, applicants must show that the particular range is critical, generally by showing that that claimed range achieves unexpected results. See M.P.E.P. 2144.05 III. In fact, the originally filed specification does not demonstrate any criticality and/or novelty as to why the forming gas has to be four percent.

In re claim 5, Chung et al. substantially teach the claimed method, including removing the resist layer utilizing a plasma etch but do not expressly teach providing a wet preclean after the plasma etching step (d).

However, AAPA in an analogous art teaches providing the ARC layer 52; patterning a resist layer 53; etching a first layer 51 and the ARC layer 53; and removing the resist layer 53 followed by a wet etch (page 2, lines 9-11).

Therefore, it would have been obvious to one of the ordinary skill in the art at the time of the invention was made to perform the wet preclean (i.e. wet etch) as taught by AAPA after removing the resist layer in Chung's method, since by doing so it would clean the residues from the plasma etching (page 2, lines 10-11, AAPA), which, in turn, would benefit the critical dimension of the device.

Response to Arguments

7. Applicant's arguments filed 5/23/03 have been fully considered but they are not persuasive.

Applicants argue that Chung et al. fail to disclose an ARC layer comprising a layer of SiON of less than about 500 Angstroms in thickness because Chung et al. use the ARC as a "stop layer", not ARC layer, and do not have the claimed thickness range (first paragraph, page 8).

In response to the argument, Chung et al., indeed, use the SiON layer as the stop layer. Chung et al. further suggest that the SiON layer has the **function of ARC** as well (col. 4, lines 29-31). In addition, in light of the claimed limitation " the ARC layer being resistant to the plasma etch" (claim 1, step (d)), one of the ordinary skilled in the art would have recognize that the claimed ARC layer has the function of "stop layer" as well. In other words, in terms of purpose or function, the ARC layer of Chung et al. is **exactly same** as that of the claimed ARC layer.

The only difference between the two is that Chung et al. do not teach the claimed ARC layer thickness. However, the selection of the ARC layer thickness is obvious to one of the ordinary skilled in the art, as stated above.

Furthermore, the newly added claims 13-17 are not patentably distinct from the combination of Plat et al, Chung et al. and AAPA, as stated above.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Plat to US 6,222,241 teaches at least the claimed subject matter as recited in claims 1 and 13.

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hsien-Ming Lee whose telephone number is 703-305-7341. The examiner can normally be reached on M-F (9:00 ~ 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 703-306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Hsien-Ming Lee
Examiner
Art Unit 2823

July 30, 2003

W. David Coleman
Primary Examiner